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H01L 21/768

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(54) Abstract Title

Dual damascene structure and manufacturing methods.

(57) Two methods of forming an interconnection are disclosed; both comprise implanting at least one buried etch stop layer 306, 310, 406 in a dielectric layer 302, 402 above a semiconductor substrate 300, 400. The first method (fig. 31) comprises implanting a first etch stop layer 306 having an opening using a mask (not shown), forming sidewall spacers on the mask to enable implanting a second shallower etch stop layer 310 having a wider opening and etching the dielectric in the openings of the etch stop layers. The second method (fig 4G) comprises forming a mask with sidewall spacers on the dielectric layer above the semiconductor substrate, implanting an shallow implantation stop layer, removing the sidewall spacers, implanting a deeper etch stop layer, reducing the anti-implantation ability of the implantation stop layer and etching the dielectric layer using the mask and the etch stop layer to form a trench and a via. The trenches and vias formed are then filled with a conductive material 314, 414.

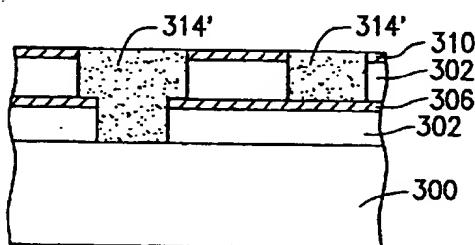


FIG. 3I

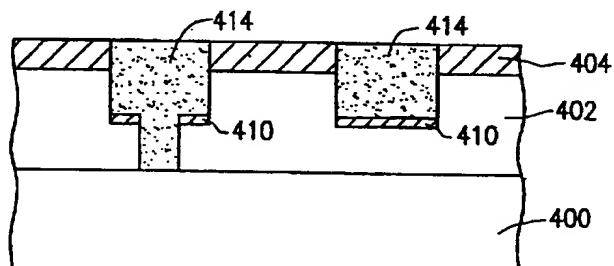


FIG. 4G

*see f. 4D*

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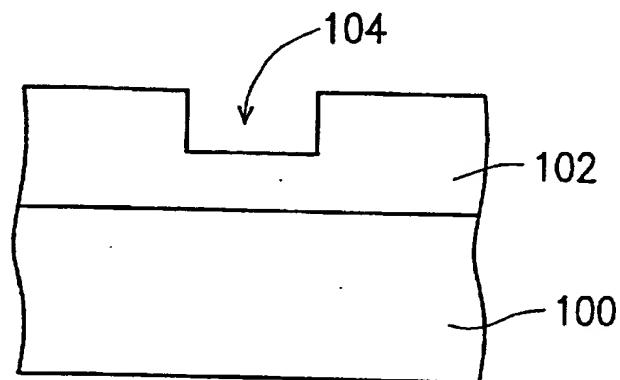


FIG. 1A (PRIOR ART)

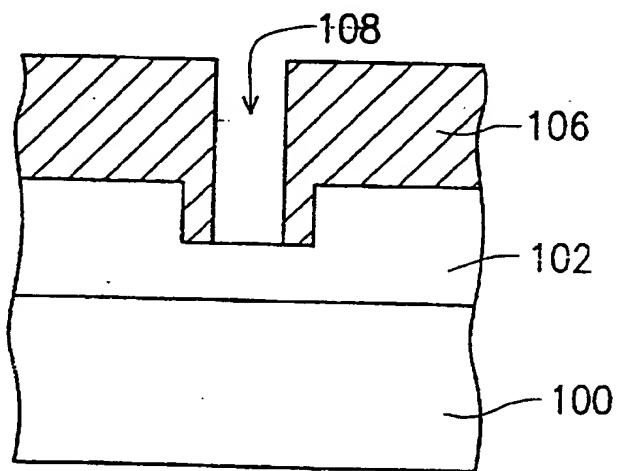


FIG. 1B (PRIOR ART)

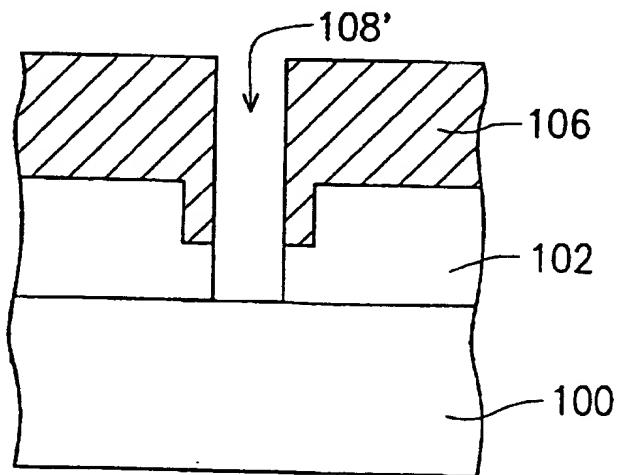


FIG. 1C (PRIOR ART)

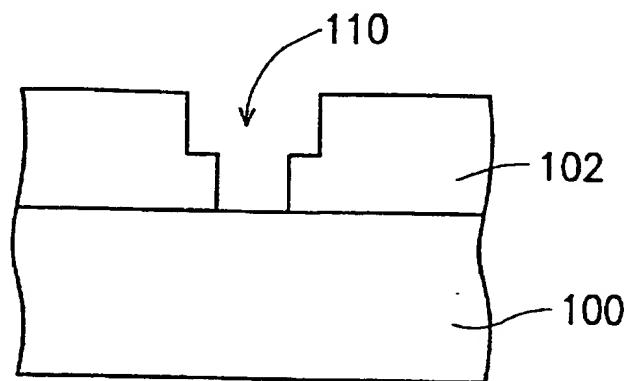


FIG. 1D (PRIOR ART)

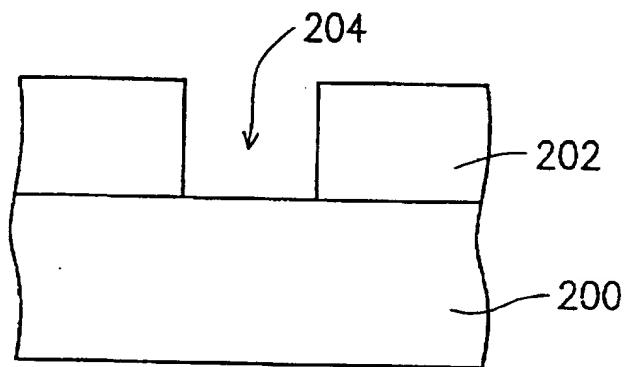


FIG. 2A (PRIOR ART)

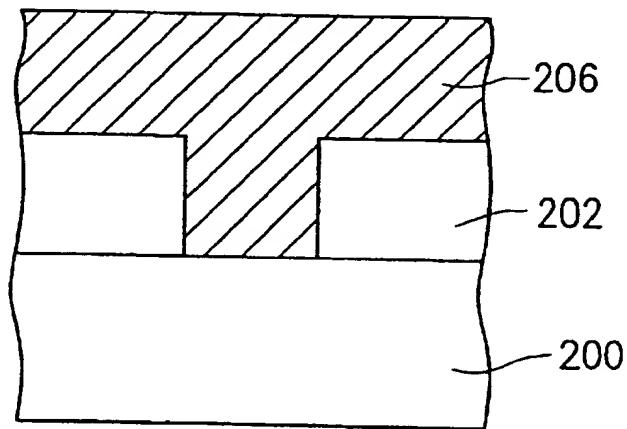


FIG. 2B (PRIOR ART)

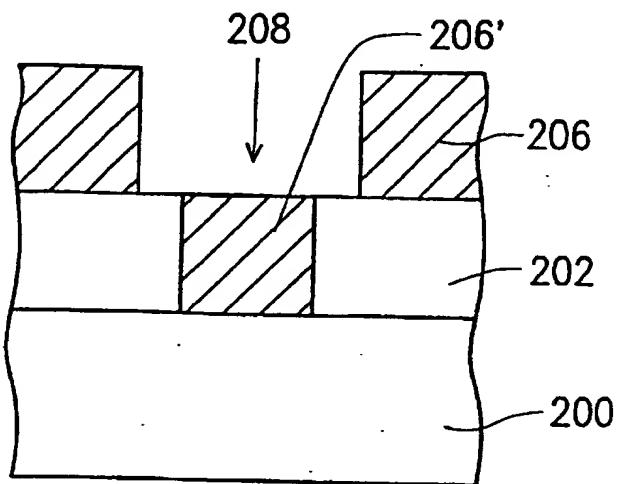


FIG. 2C (PRIOR ART)

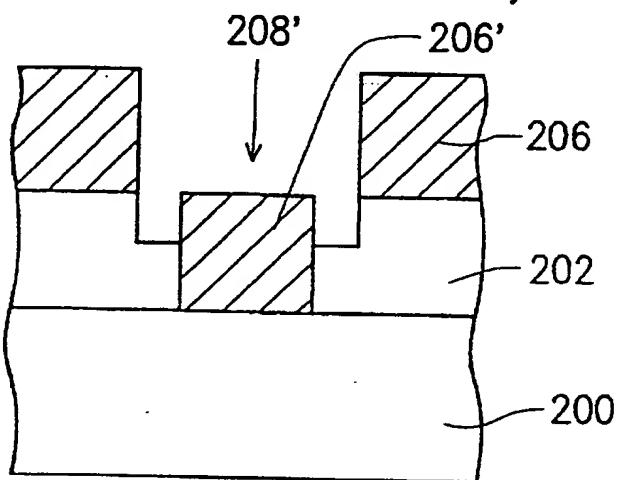


FIG. 2D (PRIOR ART)

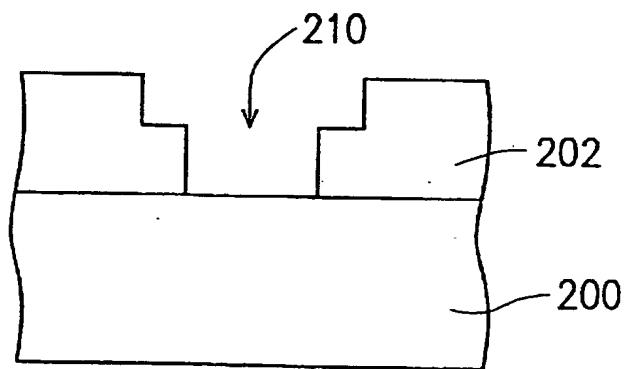


FIG. 2E (PRIOR ART)

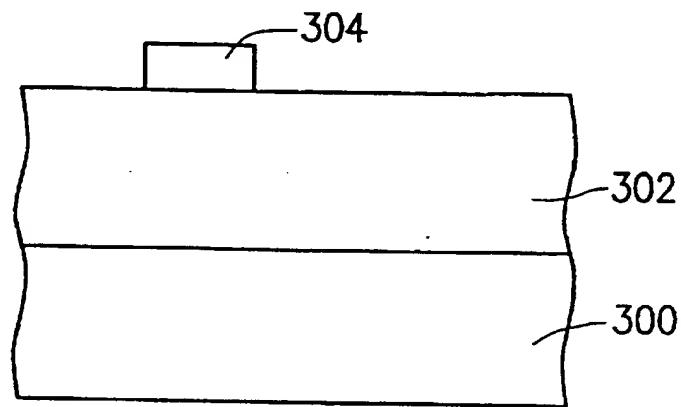


FIG. 3A

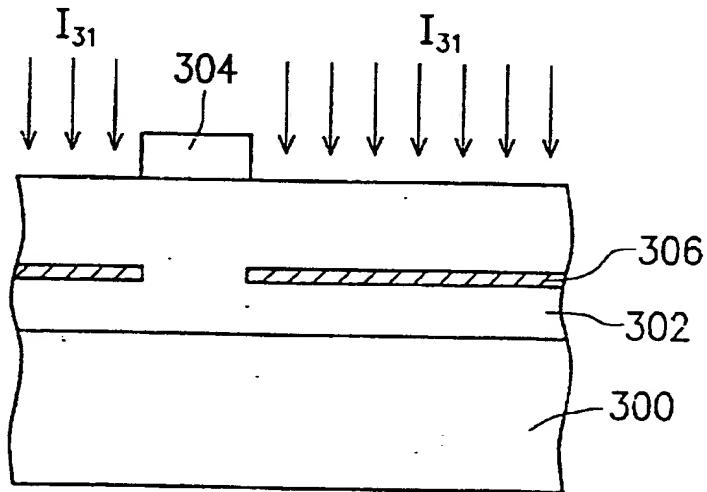


FIG. 3B

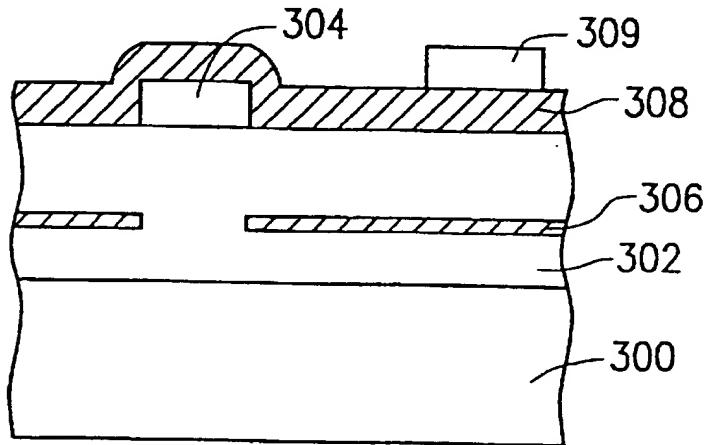


FIG. 3C

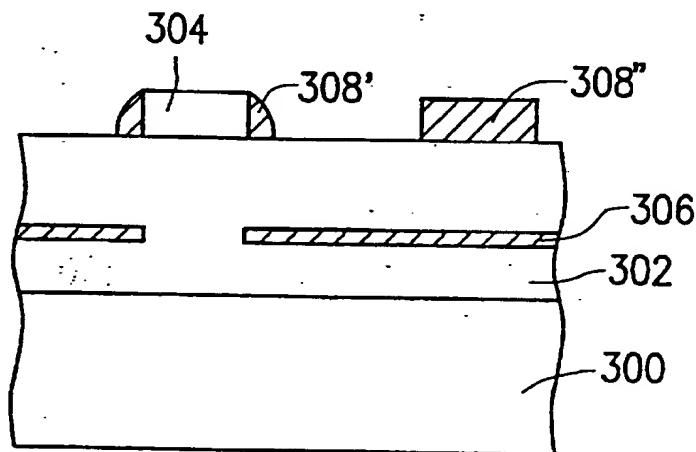


FIG. 3D

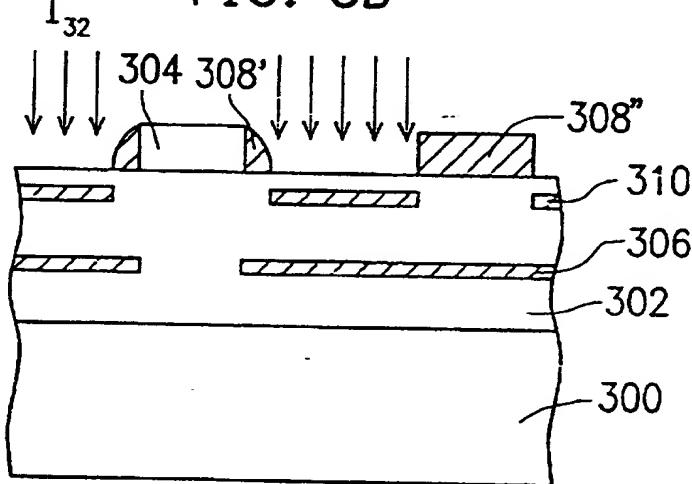


FIG. 3E

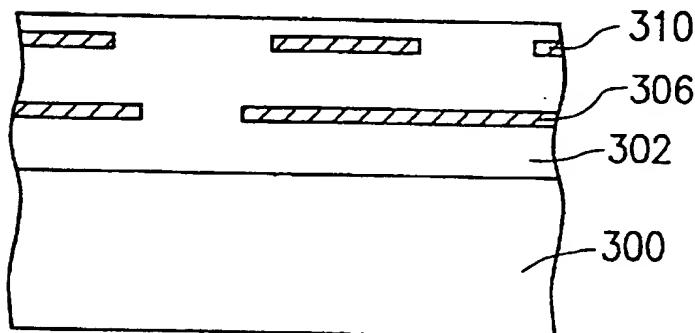


FIG. 3F

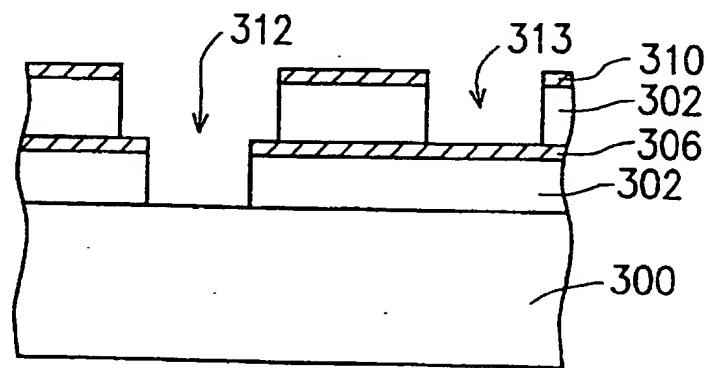


FIG. 3G

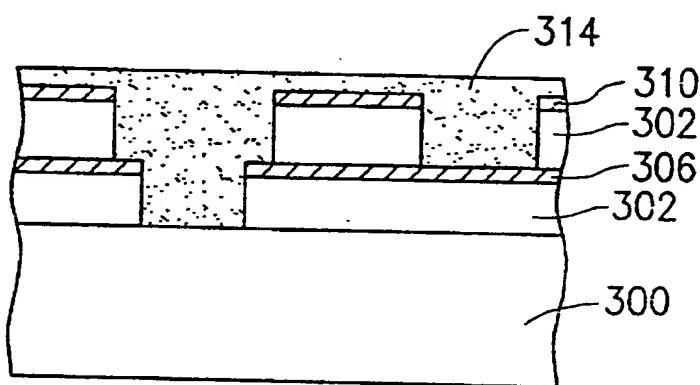


FIG. 3H

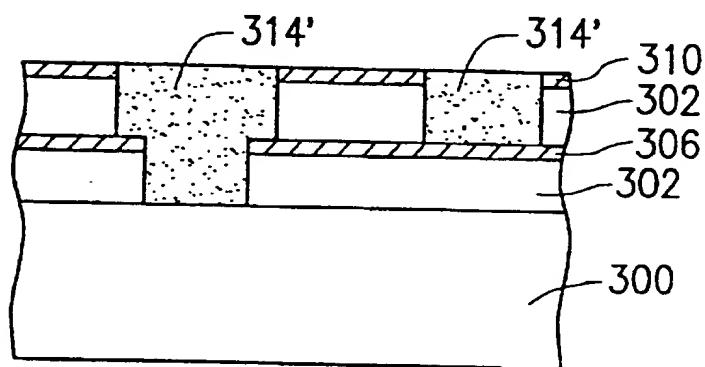


FIG. 3I

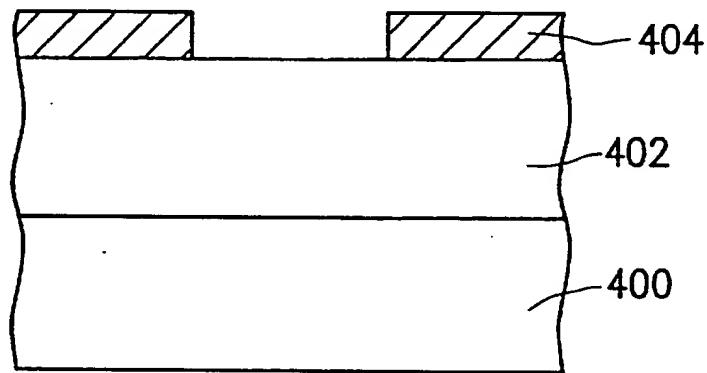


FIG. 4A

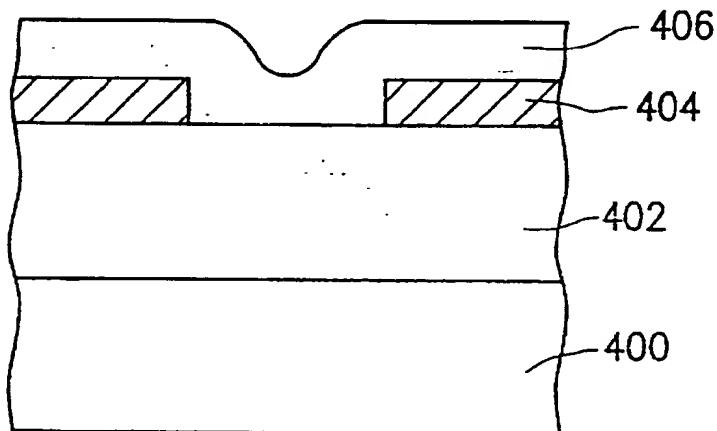


FIG. 4B

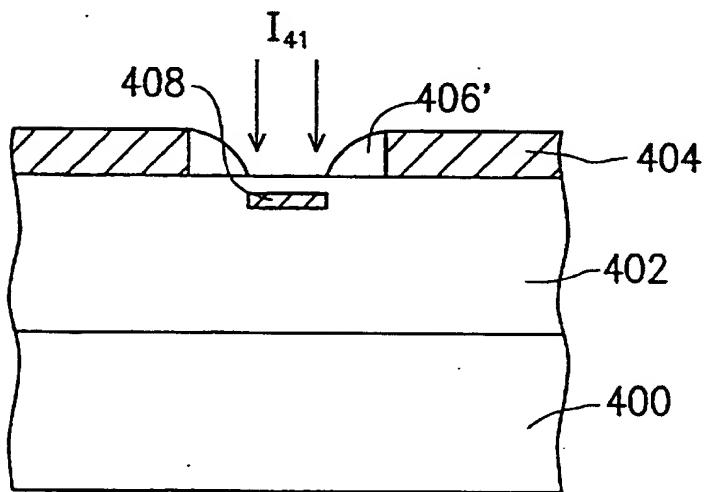


FIG. 4C

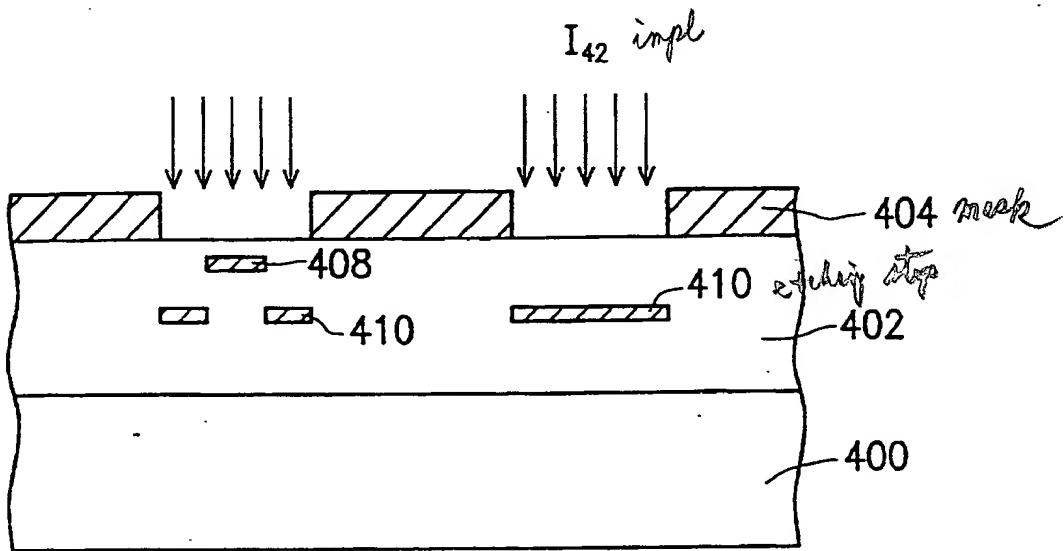


FIG. 4D

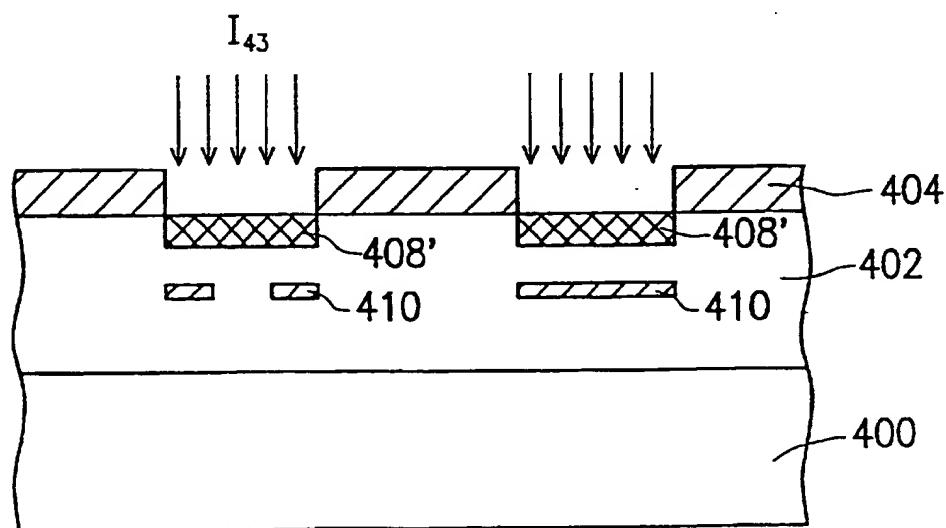


FIG. 4E

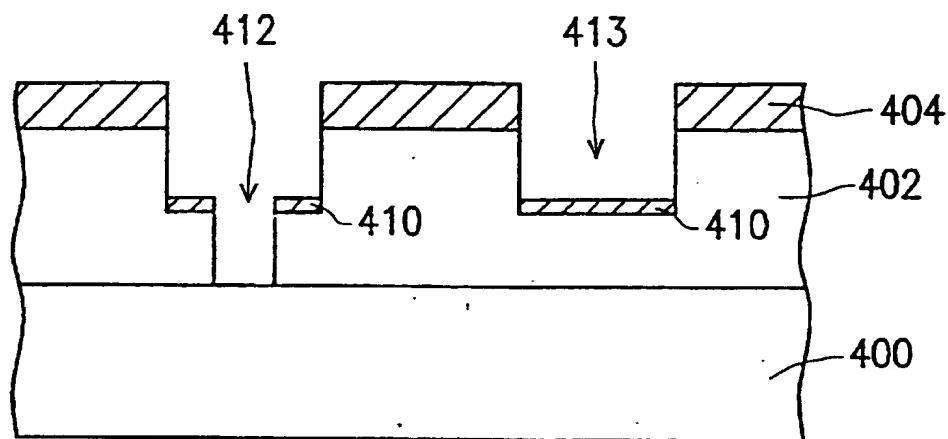


FIG. 4F

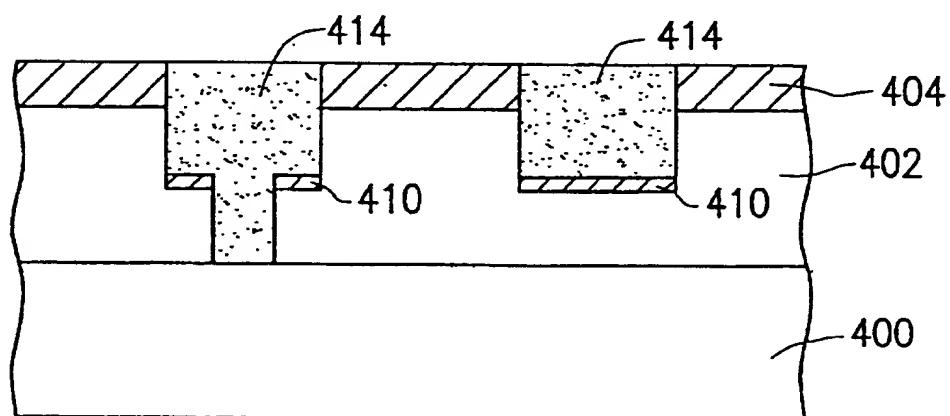


FIG. 4G

DUAL DAMASCENE STRUCTURE AND ITS  
MANUFACTURING METHOD

5

BACKGROUND OF THE INVENTION

Field of the Invention

This invention relates in general to a semiconductor component and its manufacturing method, and more particularly to a multi-level metallization and interconnection component and its manufacturing method.

10

Description of the Related Art

As the level of integration for integrated circuits increases, the number of interconnects necessary for linking up devices increases, too. Therefore, design employing two or more metallic layers is gradually becoming the norm in the fabrication 15 of integrated circuits. When the level of integration is further increased a high production yield and good reliability is difficult to get. Damascene processing method is a fabrication technique that involves the creation of interconnect lines by first etching a trench in a planar dielectric layer, and then filling that trench with metal. The method is capable of introducing copper metal which is not easily etched into the semiconductor 20 device. Therefore, this method is the best choice in the manufacturing industry for sub-quarter micron interconnects.

Conventional damascene processing technique has a number of problems. For example, depth of trench lines is hard to control, profile of via sidewall is difficult to standardize and the processing window is quite narrow.

Fig. 1A to Fig. 1D are cross-sectional views showing the manufacturing steps of a conventional dual damascene processing method. As shown in Fig. 1A, an insulator layer 102 is deposited over a semiconductor substrate 100. Then, a mask is used to define the pattern of the interconnection on the insulator layer 102. An etching process is carried out  
5 for forming a trench 104 in the insulator layer 102.

Next, referring to Fig. 1B, a thick photoresist layer 106 is formed over the insulator layer 102, filling in the trench 104. Defining and etching processes are then performed to expose the surface of the insulator layer 102 in the trench 104 so as to form a first via 108.

10 Then, as shown in Fig. 1C, an etching process is performed to remove parts of the insulator layer 102 exposed in the first via 108 and to form a second via 108', exposing the semiconductor substrate 100.

15 Next, the photoresist layer 106 is removed as shown in Fig. 1D so as to form a third via 110 with two different of widths. A conductive layer (not shown) is formed over the entire structure; thereafter a polishing process is performed to remove the conductive layer over the insulator layer 102. This completes the forming of the dual damascene structure.

The method of manufacturing the dual damascene according the conventional method described above is not without flaws. After the trench is formed, it is necessary to  
20 perform a photolithography step for forming the first via. And, the width of the first via is smaller than the trench, therefore misalignment of the pattern occurs during the defining procedure. Furthermore, it is difficult to etch and form the via owing to the larger aspect ratio of the second via.

Fig. 2A to Fig. 2E are cross-sectional views showing the manufacturing steps of another conventional dual damascene processing method. As shown in Fig. 2A, an insulator layer 202 is deposited over a semiconductor substrate 200. Then, a mask is used to define the pattern of the interconnection on the insulator layer 202. An etching process 5 is carried out to form a trench 204 within the insulator layer 202 and expose the surface of the semiconductor substrate 200.

Next, referring to Fig. 2B, a layer of photoresist 206 is formed over the insulator layer 202, filling the via 204. Then, as shown in Fig. 2C, a mask is used to define the pattern of the trench 208 within the photoresist layer 206, and the undesired photoresist 10 206 is removed to expose parts of the insulator layer 202. The photoresist plug 206' remains in the via 204. The width of the trench 208 is larger than the via 204.

Referring to Fig. 2D, an etching step is then performed on the insulator layer 202 so as to form a trench 208' by using the trench pattern 208 within the photoresist layer 206.

15 Next, as shown in Fig. 2E, the photoresist layer 206 and photoresist plug 206' are removed. A conductive layer (not shown) is formed on the entire structure; thereafter a polishing process is performed to remove the conductive layer over the insulator layer 202. This completes the forming of the dual damascene structure.

The method described above still has drawbacks. For example, there is no etching 20 stop layer within the insulator layer, therefore it may be over-etched during the trench etching operation. As the level of integration for integrated circuits increases, it is harder and harder to remove the photoresist plug within the via. Furthermore, this method also uses several photolithographic and etching steps which are accompanied by misalignment during the via and trench formation procedures.

## SUMMARY OF THE INVENTION

It is therefore an object of the invention to provide a dual damascene structure and its manufacturing method which uses a nitrogen implantation step to form an etch stop layer. The present invention improves the control of the etching stop during the etching process which is used to form the trench. In addition, the polysilicon or silicon nitride layer is used as masks for reducing misalignment during the step forming of the via and trench.

The invention achieves the above-identified objects by providing a new method of forming a dual damascene structure. A dielectric layer is formed above a semiconductor substrate. A patterned mask layer is formed on the dielectric layer. A first implanting step is performed to implant nitrogen gases or ions and a thermal annealing step is then performed so as to form a first etching stop layer in the dielectric layer. The first etching stop layer has a via opening at the position corresponding to the mask layer. A patterned photoresist layer is formed. Then, a spacer is formed on the sidewall of the photoresist layer and the spacer layer under the photoresist layer remains. A second implanting step is performed to form a second etching stop layer on the dielectric layer; the second etching stop layer has a trench opening. Thereafter, the spacer layer, spacer, and mask layer are removed. Parts of the dielectric layer are removed to form the trench and via by using an anisotropic etching step. A conductive layer is formed in the trench and via so as to form the dual damascene structure coupled to the semiconductor substrate.

The invention achieves the above-identified objects by providing another new method of forming a dual damascene structure. A dielectric layer is formed above the semiconductor substrate. A mask layer having an opening is formed on the dielectric layer. A spacer is formed on the sidewall of the opening. An implanting stop layer is

formed in the dielectric layer by performing a first implanting step to implant nitrogen ions. The implanting stop layer is formed at the position corresponding to the opening formed by the spacer. The spacer is removed, and another trench opening is formed in the mask layer. A second implanting step is performed to form an etching stop layer in the  
5 dielectric layer. The etching stop layer is formed at the position corresponding to the opening on the mask layer. A third implanting step is performed to reduce the anti-implantation ability of the implanting stop layer. The implanting stop layer is transformed into an incohesive structure or oxide-like structure. Then, an anisotropic etching step is performed to form a trench and via. The via exposes the semiconductor  
10 substrate. Finally, a conductive layer is formed in the trench and via. This completes the formation of the dual damascene structure.

#### BRIEF DESCRIPTION OF THE DRAWINGS

Other objects, features, and advantages of the invention will become apparent  
15 from the following detailed description of the preferred but non-limiting embodiments. The description is made with reference to the accompanying drawings in which:

Fig. 1A to Fig. 1D (prior art) are cross-sectional views showing the manufacturing steps of a conventional dual damascene processing method;

Fig. 2A to Fig. 2E (prior art) are cross-sectional views showing the manufacturing  
20 steps of another conventional dual damascene processing method;

Figures 3A to 3I are cross-sectional views showing the process steps of one preferred embodiment of the method for manufacturing the dual damascene.

Figures 4A to 4G are cross-sectional views showing the process steps of another preferred embodiment of the method for manufacturing the dual damascene.

## DESCRIPTION OF THE PREFERRED EMBODIMENT

Figures 3A to 3I are cross-sectional views showing the process steps of one preferred embodiment of the method for manufacturing the dual damascene.

Referring to Fig. 3A, a dielectric layer 302 is formed on a semiconductor substrate 300. There are many devices formed on the substrate, but they are not shown in order to simplify the figures. The dielectric layer 302, for example, is a silicon dioxide or borophosphosilicate glass layer, with a thickness of about 20000 Å. A layer of mask 304 is then formed on the dielectric layer 302.

Next, referring to Fig. 3B, a first implanting step  $I_{31}$  is performed to implant reactants, for example, nitrogen gases or ions, into dielectric layer 302 by using the mask layer 304. Then, an annealing step at a temperature of about 350-450 °C is performed to form a first etching stop layer 306, for example, a silicon nitride layer, at a depth of about 9000-10000 Å. The range of the annealing temperature is controlled so it does not affect the diffusion of the implants. The U.S. patent No. 5,314,843 discloses an implanting method regarding control of the implanting energy to implant reactants into the determined depth with a determined concentration.

Thereafter, referring to Fig. 3C, after the first etching stop layer 306 is formed, a layer of spacer 308, for example, titanium nitride or polysilicon spacer, is formed, for example, by chemical vapor deposition method, over the dielectric layer 302 and the mask layer 304. Then, a layer of photoresist 309 is formed over the spacer 308.

Next, referring to Fig. 3D, parts of the spacer layer 308 and photoresist layer 309 are removed until the top surface of the mask layer 304 is exposed so as to form a spacer 308' on the sidewall of the mask 304 and to leave a spacer 308'' under the second

photoresist layer 309. The first photoresist layer 304, spacer 308', and spacer 308'' constitute a trench mask.

As shown in Fig. 3E, a second implanting is performed to implant reactants, for example, nitrogen ions, into the dielectric layer 302. Then, an annealing step at a 5 temperature of about 350-450 °C is performed to form a second etching stop layer 310, for example, a silicon nitride layer, with the depth of about 1000-2000 Å by using the trench mask. Referring again to the U.S. patent No. 5,314,843, an implanting method is disclosed regarding control of the implanting energy to implant reactants into the determined depth at a determined concentration.

10 Next, referring to Fig. 3F, the trench mask is removed. The first etching stop layer 306 and second etching stop layer 310 are formed within the dielectric layer 302. The first etching stop layer 306 has an opening which is used to form a via, and the second etching stop layer 310 has an opening which is used to form a trench. The size of the opening in the first etching stop layer 306 corresponds to the mask layer 304, and the size 15 of the opening in the second etching stop layer 310 corresponds to the size of the opening in the trench mask. Therefore the size of the trench is larger than the via.

Referring to Fig. 3G, parts of the dielectric layer 302 are removed, for example, by using an anisotropic etching method and using the first and second etching stop layers 306 and 310 as stop layers for protecting the underneath dielectric layer 302 from etching. 20 Furthermore, the first and second etching layer 306 and 310 have openings; therefore the trench/via 312 and trench 313 are formed during the etching process. Additionally, the substrate is exposed by the via 312.

Next, referring to Fig. 3H, a conductive layer 314 is formed over the structure illustrated in Fig. 3G. The conductive layer 314 is made of metal, for example, copper, aluminum, aluminum alloy or aluminum-copper alloy.

Referring to Fig. 3I, the conductive layer 314 over the second etching stop layer 5 310 is removed, for example, by chemical mechanical polishing method, so as to form an interconnect structure 314' in the trench/via 312 and trench 313. This completes the forming of the dual damascene structure.

Figures 4A to 4G are cross-sectional views showing the process steps of another preferred embodiment of the method for manufacturing the dual damascene.

10 First, referring to Fig. 4A, a dielectric layer 402 is formed on a semiconductor substrate 400. There are many devices formed on the substrate, but they are not shown in order to simplify the figures. The dielectric layer 402 is, for example, a silicon dioxide or borophosphosilicate glass layer, with a thickness of about 20000 Å. A layer of mask 404 with an opening is formed on the dielectric layer 402.

15 Next, referring to Fig. 4B, a layer of spacer 406, for example, titanium nitride or polysilicon, is formed, for example, by using a chemical vapor deposition method, over the structure illustrated in Fig. 4A.

As shown in Fig. 4C, parts of the spacer 406 are removed, for example, by using an etching back method, to form a spacer 406' on the sidewall of the mask layer 404 in the 20 opening. Then, a first implanting step I<sub>a1</sub> is performed for implanting reactants, for example, nitrogen ions, into the dielectric layer 402 to form a implanting stop layer 408, for example, a silicon nitride layer, with a depth of about 1000-2000 Å by using the mask layer 404 and spacer 406'. The U.S. patent No. 5,314,843 discloses an implanting method regarding control of the implanting energy to implant reactants into the

determined depth at a determined concentration. The size of the implanting stop layer 408 is the same as the opening formed in the spacer 406' and mask layer 404.

Next, referring to Fig. 4D, the spacer 406' is removed and then another defining step is performed to form a trench opening in the mask layer 406'. A second 5 implanting process  $I_{42}$  is performed to implant reactants, for example, nitrogen ions, into the dielectric layer 402. Then, an annealing process with a higher temperature is performed to form an etching stop layer 410, for example, a silicon nitride layer, with a depth of about 9000-10000 Å. Referring again to the U.S. patent No. 5,314,843, it discloses an implanting method regarding control of the implanting energy to implant 10 reactants at a determined depth with a determined concentration. Because the implanting stop layer 408 and mask layer 404 can be used as barrier layers during the second implanting process  $I_{42}$ , the etching stop layer 410 is not formed behind the implanting stop layer 408 and mask layer 404.

Then, referring to Fig. 4E, a third implanting step  $I_{43}$  is performed to transform the 15 implanting stop layer 408 into an incohesive structure 408', for example, by implanting oxygen gases into the implanting stop layer 408 without performing the high temperature annealing step, but so that a dielectric layer 402-like layer is formed during the high temperature annealing step. This third implanting step  $I_{43}$  destroys the crystal of the silicon nitride or reduces the silicon nitride layer into the oxide-like structure. It therefore 20 undoes the barrier ability of the implanting stop layer 408.

Thereafter, referring to Fig. 4F, parts of the dielectric layer 402 are removed, for example, by using an anisotropic etching method, so as to exposes the semiconductor substrate 400 by using the mask layer 404 and etching stop layer 410 as barrier layers.

Therefore, the dielectric layer 402 under the mask layer 404 and etching stop layer 410 aren't be removed, and finally a trench/via 412 and a trench 413 are formed.

Next, as shown in Fig. 4G, a conductive layer, for example, a metal layer, is formed over the structure as shown in Fig. 4F. The material used for the conductive layer 5 can be copper, aluminum, aluminum alloy or aluminum-copper alloy. The conductive layer over the mask layer 404 is removed, for example, by using a chemical mechanical polishing method, to form an interconnection structure 414 in the trench/via 412 and trench 413. This completes the forming of the dual damascene structure.

The characteristic of the present invention includes using two implanting step to 10 form the two etching stop layer within the dielectric layer. The invention does not have difficulty in controlling the etching stop, as does the prior art.

Another characteristic of the present invention is that of providing a dual damascene structure and its manufacturing method. The present invention uses the spacer as the trench mask, but two mask are used in the prior art. The misalignment of the 15 conventional method doesn't occurred in the present invention.

While the invention has been described by way of example and in terms of a preferred embodiment, it is to be understood that the invention is not limited thereto. To the contrary, it is intended to cover various modifications and similar arrangements and procedures, and the scope of the appended claims therefore should be accorded the 20 broadest interpretation so as to encompass all such modifications and similar arrangements and procedures.

## WHAT IS CLAIMED IS:

1. A dual damascene structure comprising:
  - a semiconductor substrate;
  - a dielectric layer formed above the semiconductor substrate;
  - 5 a first etching stop layer formed in the dielectric layer, the first etching stop layer having a first opening;
  - a second etching stop layer formed on the dielectric layer, the second etching stop layer having a second opening formed at the position corresponding to the first opening of the first etching stop layer; and
- 10 an interconnection structure formed in the dielectric layer, first etching stop layer, and second etching stop layer.
2. A dual damascene structure according to claim 1, wherein the thickness of the dielectric layer is about 20000 Å.
3. A dual damascene structure according to claim 1, wherein the dielectric layer 15 comprises silicon dioxide.
4. A dual damascene structure according to claim 1, wherein the dielectric layer comprises borophosphosilicate glass.
5. A dual damascene structure according to claim 1, wherein the dielectric layer comprises low dielectric materials.
- 20 6. A dual damascene structure according to claim 1, wherein the first etching stop layer is formed in the dielectric layer with a depth of about 10000 Å down from the surface of the semiconductor substrate.
7. A dual damascene structure according to claim 1, wherein the first etching stop layer is a silicon nitride layer.

8. A dual damascene structure according to claim 7, wherein the silicon nitride layer is formed by implanting reactants into the dielectric layer and performing an annealing step.

9. A dual damascene structure according to claim 8, wherein the reactants  
5 comprise nitrogen/nitrogen ions.

10. A dual damascene structure according to claim 8, wherein the temperature of the annealing step is about 350-450 °C.

11. A dual damascene structure according to claim 1, wherein the second etching stop layer is higher than the first etching stop layer, at about 8000 Å.

10 12. A dual damascene structure according to claim 11, wherein the second etching stop layer is a silicon nitride layer.

13. A dual damascene structure according to claim 12, wherein the silicon nitride layer is formed by implanting nitrogen/nitrogen ions into the dielectric layer and performing a reaction.

15 14. A dual damascene structure according to claim 1, wherein the size of the second opening is larger than the first opening.

15. A dual damascene structure comprising :  
a semiconductor substrate;  
a dielectric layer formed above the semiconductor substrate;  
20 a first silicon nitride layer formed in the dielectric layer, the first silicon nitride layer having a first opening, the first silicon nitride layer being formed by implanting the first reactants into the dielectric layer and performing a first annealing step; and  
a second silicon nitride layer formed on the dielectric layer, the second silicon nitride layer having a second opening at the position corresponding to the first opening of

the first silicon nitride layer, the second silicon nitride layer being formed by implanting the second reactants into the dielectric layer and performing a second annealing step, wherein the size of the second opening is larger than first opening.

16. A dual damascene structure according to claim 15, wherein the thickness of  
5 the dielectric layer is about 20000 Å.

17. A dual damascene structure according to claim 15, wherein the dielectric layer comprises silicon dioxide.

18. A dual damascene structure according to claim 15, wherein the dielectric layer comprises borophosphosilicate glass.

10 19. A dual damascene structure according to claim 15, wherein the dielectric layer comprises low dielectric materials.

20. A dual damascene structure according to claim 15, wherein the first silicon nitride layer is formed in the dielectric layer with a depth about 10000 Å down from the surface of the semiconductor substrate.

15 21. A dual damascene structure according to claim 15, wherein the first reactants comprise nitrogen/nitrogen ions.

22. A dual damascene structure according to claim 15, wherein the temperature of the first annealing step is about 350-450 °C .

23. A dual damascene structure according to claim 15, wherein the second reactants comprise nitrogen/nitrogen ions.

24. A dual damascene structure according to claim 15, wherein the temperature of the second annealing step is about 350-450 °C .

25. A dual damascene structure according to claim 15, wherein the second silicon nitride layer is higher than the first etching stop layer about 8000 Å.

26. A method of forming a dual damascene structure, comprising the steps of:

- providing a semiconductor substrate;
- forming a dielectric layer above the semiconductor substrate;
- forming a patterned mask layer on the dielectric layer;
- 5 performing a first implanting step to form a first etching stop layer in the dielectric layer, the first etching stop layer having a via opening;
- forming a spacer layer on the mask layer;
- forming a patterned photoresist layer on the spacer layer;
- removing parts of the photoresist and spacer layer so as to form a spacer on the
- 10 sidewall of the mask layer and to leave the spacer layer under the photoresist layer;
- performing a second implanting step to form a second etching stop layer on the dielectric layer, the second etching stop layer having a trench opening;
- removing the spacer layer, spacer, and mask layer;
- removing parts of the dielectric layer to expose parts of the semiconductor
- 15 substrate, first etching stop layer and second etching stop layer;
- forming a conductive layer on the semiconductor substrate, first etching stop layer and second etching stop layer; and
- removing the conductive layer above the second etching stop layer so as to form the dual damascene structure.

20 27. A method according to claim 26, wherein the thickness of the dielectric layer is about 20000 Å.

28. A method according to claim 26, wherein the dielectric layer comprises silicon dioxide.

29. A method according to claim 26, wherein the dielectric layer comprises borophosphosilicate glass.

30. A method according to claim 26, wherein the dielectric layer comprises low dielectric materials.

5 31. A method according to claim 26, wherein the first etching stop layer is formed in the dielectric layer with a depth of about 10000 Å down from the surface of the semiconductor substrate.

32. A method according to claim 26, wherein the first etching stop layer is a silicon nitride layer.

10 33. A method according to claim 32, wherein the silicon nitride layer is formed by implanting reactants into the dielectric layer and performing an annealing step.

34. A method according to claim 33, wherein the reactants comprise nitrogen/nitrogen ions.

15 35. A method according to claim 33, wherein the temperature of the annealing step is about 350-450 °C.

36. A method according to claim 26, wherein the second etching stop is higher than the first etching stop layer, at about 8000 Å.

37. A method according to claim 26, wherein the second etching stop layer is a silicon nitride layer.

20 38. A method according to claim 37, wherein the silicon nitride layer is formed by implanting reactants into the dielectric layer.

39. A method according to claim 38, wherein the reactants comprise nitrogen/nitrogen ions.

40. A method according to claim 38, wherein the temperature of the annealing step is about 350-450 °C.

41. A method according to claim 26, wherein the spacer comprises polysilicon.

42. A method according to claim 26, wherein the spacer comprises titanium nitride.

43. A method according to claim 26, wherein the mask layer and parts of the spacer layer removing step comprise using an etching back method.

44. A method according to claim 26, wherein the second etching stop layer removing step comprises using a chemical mechanical polishing method.

45. A dual damascene structure comprising:

a semiconductor substrate;

a dielectric layer formed above the semiconductor substrate;

a via formed in the dielectric layer and exposing the semiconductor substrate;

a trench formed in the dielectric layer;

an etching stop layer formed at the interface of trench and the dielectric layer; and  
an interconnection structure formed in the trench and via.

46. A dual damascene structure according to claim 45, wherein the thickness of the dielectric layer is about 20000 Å.

47. A dual damascene structure according to claim 45, wherein the dielectric layer comprises silicon dioxide.

48. A dual damascene structure according to claim 45, wherein the dielectric layer comprises borophosphosilicate glass.

49. A dual damascene structure according to claim 45, wherein the dielectric layer comprises low dielectric materials.

50. A dual damascene structure according to claim 45, wherein the etching stop layer is a silicon nitride layer.

51. A dual damascene structure according to claim 50, wherein the silicon nitride layer is formed by implanting reactants into the dielectric layer and performing an annealing step.

52. A dual damascene structure according to claim 51, wherein the reactants comprise nitrogen/nitrogen ions.

53. A dual damascene structure according to claim 51, wherein the temperature of the annealing step is about 350–450 °C.

10 54. A method of forming a dual damascene structure, comprising the steps of:

providing a semiconductor substrate;

forming a dielectric layer above the semiconductor substrate;

forming a mask layer having a first opening on the dielectric layer;

forming a spacer on the sidewall of the first opening;

15 performing a first implanting step to form an implanting stop layer in the dielectric layer with a first depth away from the top surface of the dielectric layer;

removing the spacer, and defining a second opening in the mask layer;

performing a second implanting step to form an etching stop layer in the dielectric layer with a second depth away from the top surface of the dielectric layer;

20 performing a third implanting step to reduce the anti-implantation ability of the implanting stop layer;

removing parts of the dielectric to form a trench and a via, the via exposing the semiconductor substrate;

forming a conductive layer in the trench and via, and on the dielectric layer; and

removing the conductive layer and the mask layer on the dielectric layer.

55. A method according to claim 54, wherein the dielectric layer comprises silicon dioxide.

56. A method according to claim 54, wherein the dielectric layer comprises borophosphosilicate glass.

57. A method according to claim 54, wherein the dielectric layer comprises low dielectric materials.

58. A method according to claim 54, wherein the spacer forming step comprises the following substeps:

10 forming a spacer layer on the semiconductor substrate; and  
removing parts of the spacer layer to form the spacer on the sidewall of the opening.

59. A method according to claim 58, wherein the spacer layer comprises polysilicon.

15 60. A method according to claim 58, wherein the spacer layer comprises titanium nitride.

61. A method according to claim 58, wherein the parts of the spacer layer removing step comprise using an etching back method.

62. A method according to claim 54, wherein the implanting stop layer comprises 20 silicon nitride.

63. A method according to claim 62, wherein the silicon nitride layer is formed by implanting reactants into the dielectric layer and performing an annealing step.

64. A method according to claim 63, wherein the reactants comprise nitrogen/nitrogen ions.

65. A method according to claim 64, wherein the temperature of the annealing step is about 350-450 °C.

66. A method according to claim 54, wherein the second etching stop layer is a silicon nitride layer.

5 67. A method according to claim 66, wherein the silicon nitride layer is formed by implanting reactants into the dielectric layer and performing an annealing step.

68. A method according to claim 67, wherein the reactants comprise nitrogen/nitrogen ions.

10 69. A method according to claim 67, wherein the temperature of the annealing step is about 350-450 °C.

70. A method according to claim 54, wherein the first depth is less than the second depth.

71. A method according to claim 54, wherein the thickness of the dielectric layer is about 20000 Å.

15 72. A method according to claim 54, wherein the first depth is about 1000-2000 Å.

73. A method according to claim 54, wherein the second depth is about 10000 Å.

74. A method according to claim 54, wherein the third implanting step comprises implanting oxygen gases into the position corresponding to the implanting stop layer so 20 as to transform the implanting stop layer into an incohesive structure.

75. A method according to claim 54, wherein the third implanting step comprises implanting oxygen gases into the position corresponding to the implanting stop layer and performing an annealing step so as to transform the implanting stop layer into an oxide-like structure.

76. A method according to claim 54, wherein parts of the conductive layer and mask layer removing step comprise using a chemical mechanical polishing.

77. A dual damascene structure, substantially as hereinbefore described with reference to and/or substantially as illustrated in any one of or any combination of Figs. 3A to 4G of the accompanying drawings.

78. A method of forming a dual damascene structure, substantially as hereinbefore described with reference to and/or substantially as illustrated in any one of or any combination of Figs. 3A to 4G of the accompanying drawings.

**Amendments to the claims have been filed as follows**

1. A dual damascene structure comprising:
  - a semiconductor substrate;
  - a dielectric layer formed above the semiconductor substrate;
  - 5 a first etching stop layer formed in the dielectric layer, the first etching stop layer having a first opening;
  - a second etching stop layer formed in the dielectric layer, the second etching stop layer having a second opening formed at the position corresponding to the first opening of the first etching stop layer; and
  - 10 an interconnection structure formed in the dielectric layer, first etching stop layer, and second etching stop layer.
2. A dual damascene structure according to claim 1, wherein the thickness of the dielectric layer is about 20000 Å.
- 15 3. A dual damascene structure according to claim 1 or 2, wherein the dielectric layer comprises silicon dioxide.
4. A dual damascene structure according to claim 1 or 2, wherein the dielectric layer comprises borophosphosilicate glass.
5. A dual damascene structure according to claim 1 or 2, wherein the dielectric 20 layer comprises low dielectric materials.
6. A dual damascene structure according to any one of claims 1 to 5, wherein the first etching stop layer is formed in the dielectric layer with a depth of about 10000 Å down from the surface of the dielectric layer.
7. A dual damascene structure according to any one of claims 1 to 6, wherein 25 the first etching stop layer is a silicon nitride layer.

8. A dual damascene structure according to claim 7, wherein the silicon nitride layer is formed by implanting reactants into the dielectric layer and performing an annealing step.
9. A dual damascene structure according to claim 8, wherein the reactants 5 comprises nitrogen/nitrogen ions.
10. A dual damascene structure according to claim 8 or 9, wherein the temperature of the annealing step is about 350-450 °C.
11. A dual damascene structure according to any one of claims 1 to 10, wherein the second etching stop layer is higher than the first etching stop layer, by about 10 8000 Å.
12. A dual damascene structure according to claim 11, wherein the second etching stop layer is a silicon nitride layer.
13. A dual damascene structure according to claim 12, wherein the silicon nitride layer is formed by implanting nitrogen/nitrogen ions into the dielectric layer and 15 performing a reaction.
14. A dual damascene structure according to any one of claims 1 to 13, wherein the size of the second opening is larger than the first opening.
15. A dual damascene structure comprising:
  - a semiconductor substrate;
  - 20 a dielectric layer formed above the semiconductor substrate;
  - a first silicon nitride layer formed in the dielectric layer, the first silicon nitride layer having a first opening, the first silicon nitride layer being formed by implanting first reactants into the dielectric layer and performing a first annealing step; and
  - 25 a second silicon nitride layer formed in the dielectric layer, the second silicon

nitride layer having a second opening at the position corresponding to the first opening of the first silicon nitride layer, the second silicon nitride layer being formed by implanting second reactants into the dielectric layer and performing a second annealing step, wherein the size of the second opening is larger than first opening.

- 5    16.    A dual damascene structure according to claim 15, wherein the thickness of the dielectric layer is about 20000 Å.
17.    A dual damascene structure according to claim 15 or 16, wherein the dielectric layer comprises silicon dioxide.
18.    A dual damascene structure according to claim 15, 16 or 17, wherein the dielectric layer comprises borophosphosilicate glass.
19.    A dual damascene structure according to claim 15, 16 or 17, wherein the dielectric layer comprises low dielectric materials.
20.    A dual damascene structure according to claim 15, 16, 17, 18 or 19, wherein the first silicon nitride layer is formed in the dielectric layer with a depth about 15    10000 Å down from the surface of the dielectric layer.
21.    A dual damascene structure according to any one of claims 15 to 20, wherein the first reactants comprise nitrogen/nitrogen ions.
22.    A dual damascene structure according to any one of claims 15 to 21, wherein the temperature of the first annealing step is about 350-450 °C.
- 20    23.    A dual damascene structure according to any one of claims 18 to 22, wherein the second reactants comprise nitrogen/nitrogen ions.
24.    A dual damascene structure according to any one of claims 15 to 23, wherein the temperature of the second annealing step is about 350-450 °C.

25. A dual damascene structure according to any one of claims 15 to 24, wherein the second silicon nitride layer is higher than the first silicon nitride layer by about 8000 Å.

26. A method of forming a dual damascene structure, comprising the steps of:

5       providing a semiconductor substrate;

          forming a dielectric layer above the semiconductor substrate;

          forming a patterned mask layer on the dielectric layer;

          performing a first implanting step to form a first etching stop layer in the dielectric layer, the first etching stop layer having a via opening;

10      forming a spacer layer on the mask layer;

          forming a patterned photoresist layer on the spacer layer;

          removing parts of the photoresist and spacer layer so as to form a spacer on the sidewall of the mask layer and to leave the spacer layer under the photoresist layer;

15      performing a second implanting step to form a second etching stop layer in the dielectric layer , the second etching stop layer having a trench opening;

          removing the spacer layer, spacer, and mask layer;

          removing parts of the dielectric layer to expose parts of the semiconductor substrate, first etching stop layer and second etching stop layer;

20      forming a conductive layer on the semiconductor substrate, first etching stop layer and second etching stop layer; and

          removing the conductive layer above the second etching stop layer so as to form the dual damascene structure.

27. A method according to claim 26, wherein the thickness of the dielectric layer

25      is about 20000 Å.

28. A method according to claim 26 or 27, wherein the dielectric layer comprises silicon dioxide.
29. A method according to claim 26 or 27, wherein the dielectric layer comprises borophosphosilicate glass.
- 5 30. A method according to claim 26 or 27, wherein the dielectric layer comprises low dielectric materials.
31. A method according to claim 26, 27, 28, 29 or 30, wherein the first etching stop layer is formed in the dielectric layer with a depth of about 10000 Å down from the surface of the dielectric layer.
- 10 32. A method according to any one of claims 26 to 31, wherein the first etching stop layer is a silicon nitride layer.
33. A method according to claim 32, wherein the silicon nitride layer is formed by implanting reactants into the dielectric layer and performing an annealing step.
34. A method according to claim 33, wherein the reactants comprise
- 15 nitrogen/nitrogen ions.
35. A method according to claim 33 or 34, wherein the temperature of the annealing step is about 350-450 °C.
36. A method according to any one of claims 26 to 35, wherein the second etching stop is higher than the first etching stop layer, by about 8000 Å.
- 20 37. A method according to any one of claims 26 to 36, wherein the second etching stop layer is a silicon nitride layer.
38. A method according to claim 37, wherein the silicon nitride layer is formed by implanting reactants into the dielectric layer.
39. A method according to claim 38, wherein the reactants comprise
- 25 nitrogen/nitrogen ions.

40. A method according to claim 38 or 39, wherein the temperature of the annealing step is about 350-450 °C.
41. A method according to any one of claims 26 to 40, wherein the spacer comprises polysilicon.
- 5 42. A method according to any one of claims 26 to 40, wherein the spacer comprises titanium nitride.
43. A method according to any one of claims 26 to 42, wherein the mask layer and parts of the spacer layer removing step comprise using an etching back method.
44. A method according to any one of claims 26 to 43, wherein the step of  
10 removing the conductive layer above the second etching stop layer comprises using a chemical mechanical polishing method.
45. A dual damascene structure comprising:
  - a semiconductor substrate;
  - 15 a dielectric layer formed above the semiconductor substrate;
  - an etching stop layer formed in the dielectric layer;
  - a via formed in the dielectric layer and exposing the semiconductor substrate;
  - 20 a trench formed in the dielectric layer and exposing the etch stop layer; and
  - an interconnection structure formed in the trench and via.
46. A dual damascene structure according to claim 45, wherein the thickness of  
the dielectric layer is about 20000 Å.
- 20 47. A dual damascene structure according to claim 45 or 46, wherein the dielectric layer comprises silicon dioxide.
48. A dual damascene structure according to claim 45 or 46, wherein the dielectric layer comprises borophosphosilicate glass.

49. A dual damascene structure according to claim 45 or 46, wherein the dielectric layer comprises low dielectric materials.

50. A dual damascene structure according to any one of claims 45 to 49, wherein the etching stop layer is a silicon nitride layer.

5 51. A dual damascene structure according to claim 50, wherein the silicon nitride layer is formed by implanting reactants into the dielectric layer and performing an annealing step.

52. A dual damascene structure according to claim 51, wherein the reactants comprise nitrogen/nitrogen ions.

10 53. A dual damascene structure according to claim 51 or 52, wherein the temperature of the annealing step is about 350-450°C.

54. A method of forming a dual damascene structure, comprising the steps of:

providing a semiconductor substrate;

forming a dielectric layer above the semiconductor substrate;

15 forming a mask layer having a first opening on the dielectric layer;

forming a spacer on the sidewall of the first opening;

performing a first implanting step to form an implanting stop layer in the dielectric layer with a first depth away from the top surface of the dielectric layer;

removing the spacer, and defining a second opening in the mask layer;

20 performing a second implanting step to form an etching stop layer in the dielectric layer with a second depth away from the top surface of the dielectric layer;

performing a third implanting step to reduce the anti-implantation ability of the implanting stop layer;

removing parts of the dielectric to form a trench and a via, the via exposing

25 the semiconductor substrate;

forming a conductive layer in the trench and via, and on the dielectric layer;

and

removing the conductive layer and the mask layer on the dielectric layer.

55. A method according to claim 54, wherein the dielectric layer comprises  
5 silicon dioxide.

56. A method according to claim 54, wherein the dielectric layer comprises  
borophosphosilicate glass.

57. A method according to claim 54, wherein the dielectric layer comprises low  
dielectric materials.

10 58. A method according to any one of claims 54 to 57, wherein the spacer  
forming step comprises the following substeps:

forming a spacer layer on the semiconductor substrate; and  
removing parts of the spacer layer to form the spacer on the sidewall of the  
opening.

15 59. A method according to claim 58, wherein the spacer layer comprises  
polysilicon.

60. A method according to claim 58, wherein the spacer layer comprises titanium  
nitride.

61. A method according to claim 58, wherein the parts of the spacer layer  
20 removing step comprise using an etching back method.

62. A method according to any one of claims 54 to 61, wherein the implanting  
stop layer comprises silicon nitride.

63. A method according to claim 62, wherein the silicon nitride layer is formed  
by implanting reactants into the dielectric layer and performing an annealing step.

64. A method according to claim 63, wherein the reactants comprise nitrogen/nitrogen ions.

65. A method according to claim 63 or 64, wherein the temperature of the annealing step is about 350-450 °C.

5 66. A method according to any one of claims 54 to 65, wherein the etching stop layer is a silicon nitride layer.

67. A method according to claim 66, wherein the silicon nitride layer is formed by implanting reactants into the dielectric layer and performing an annealing step.

68. A method according to claim 67, wherein the reactants comprise

10 nitrogen/nitrogen ions.

69. A method according to claim 67 or 68, wherein the temperature of the annealing step is about 350-450 °C.

70. A method according to any one of claims 54 to 69, wherein the first depth is less than the second depth.

15 71. A method according to any one of claims 54 to 70, wherein the thickness of the dielectric layer is about 20000 Å.

72. A method according to any one of claims 54 to 71, wherein the first depth is about 1000-2000 Å.

73. A method according to any of claims 54 to 72, wherein the second depth is

20 about 10000 Å.

74. A method according to any one of claims 54 to 73, wherein the third implanting step comprises implanting oxygen gases into the position corresponding to the implanting stop layer so as to transform the implanting stop layer into an incohesive structure.

25 75. A method according to any one of claims 54 to 73, wherein the third

implanting step comprises implanting oxygen gases into the position corresponding to the implanting stop layer and performing an annealing step so as to transform the implanting stop layer into an oxide-like structure.

76. A method according to any one of claims 54 to 75, wherein parts of the conductive layer and mask layer removing step comprise using a chemical mechanical polishing.
77. A dual damascene structure, substantially as hereinbefore described with reference to and/or substantially as illustrated in any one of or any combination of Figs. 3A to 4G of the accompanying drawings.
78. A method of forming a dual damascene structure, substantially as hereinbefore described with reference to and/or substantially as illustrated in any one of or any combination of Figs. 3A to 4G of the accompanying drawings.